

Fig. 1

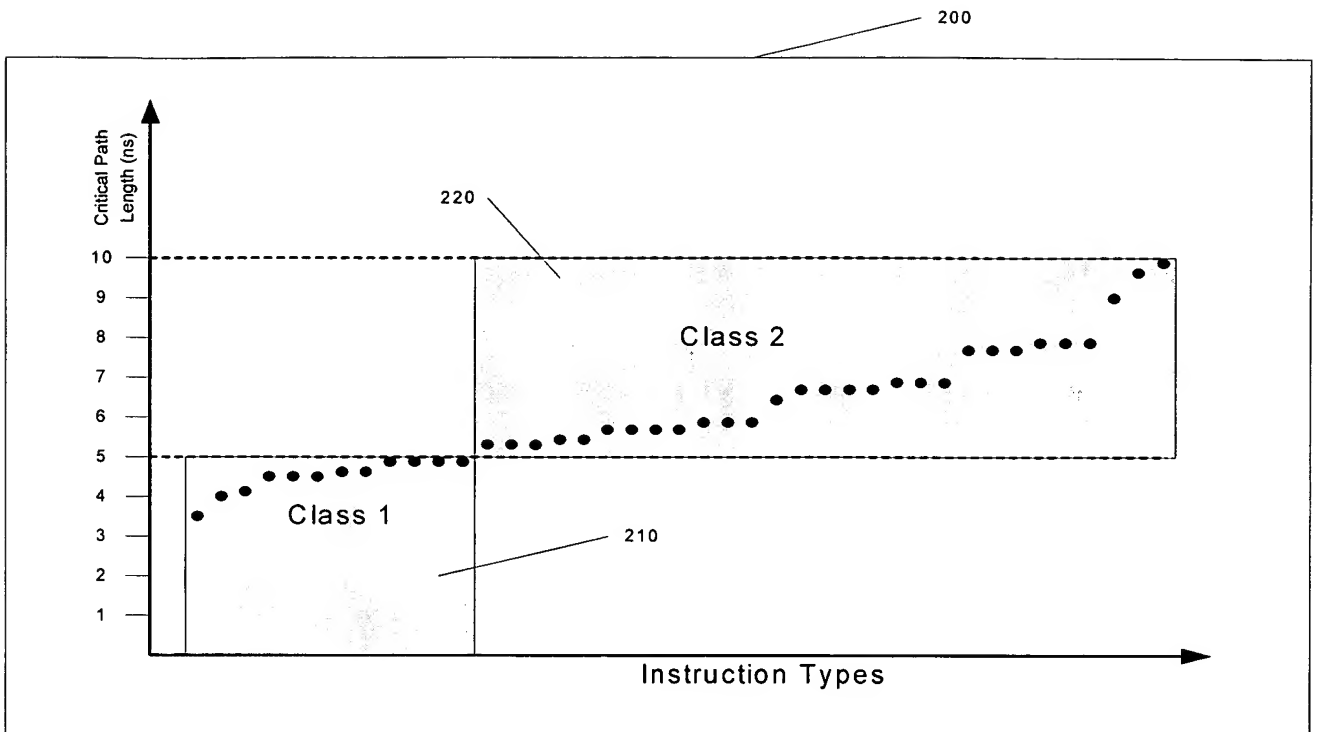


Fig. 2

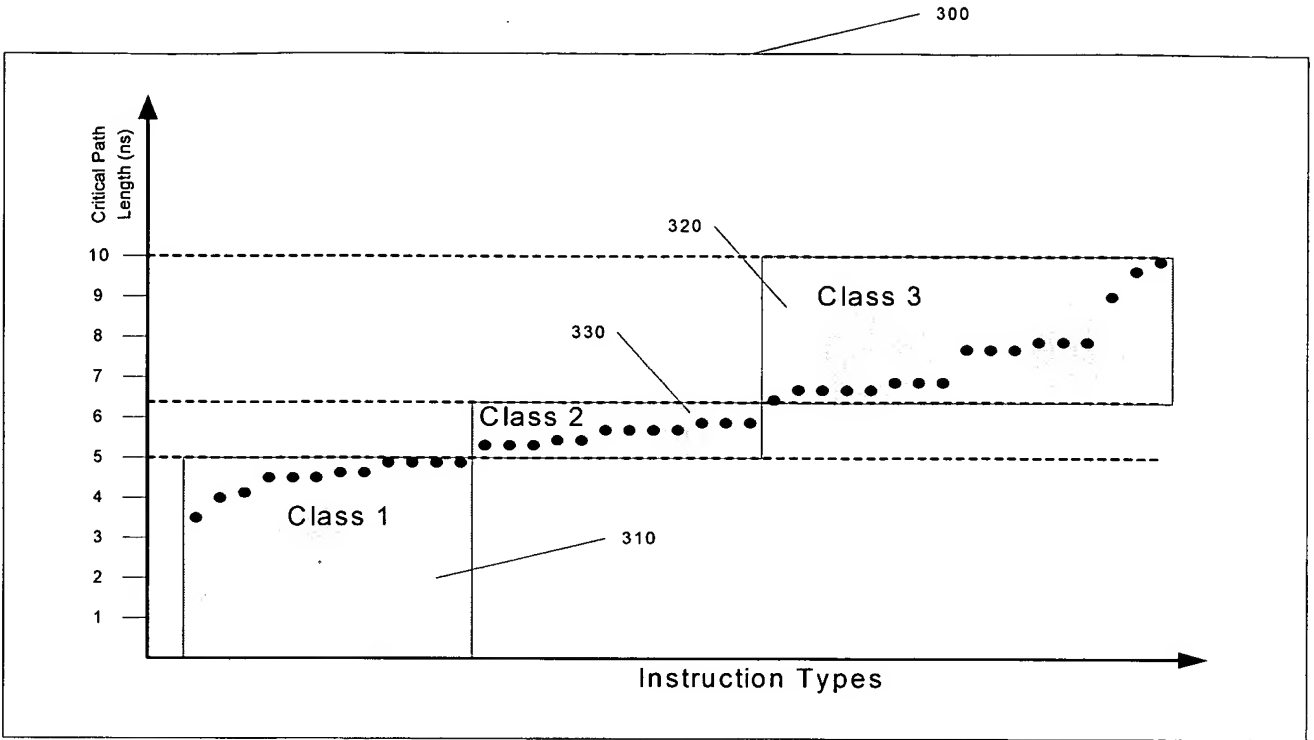


Fig. 3

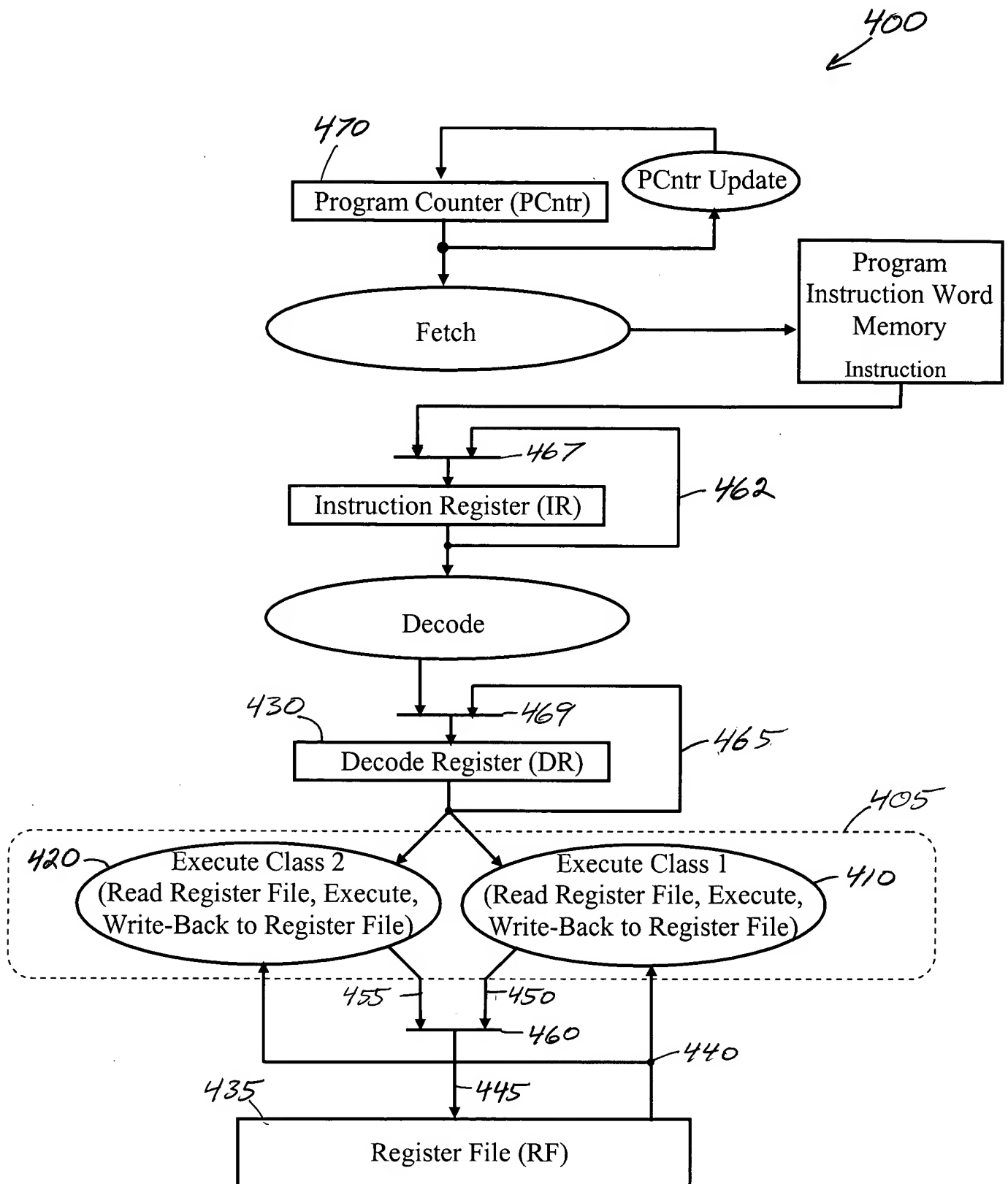


Fig. 4

500

505 MCLK Cycle #	510 Fetch	515 Decode	520 Execute
1 543	A(1) 542	:	:
2 544	B(1) 545	A(1) 546	:
3 547	C(1) 548	B(1) 549	A(1) 550
4 551	D(2) 552	C(1) 553	B(1) 554
5 555	E(1) 556	D(2) 557	C(1) 558
6 559	Hold PCntr, Hold IR 560	Hold DR 561	D(2) 562
7 563	F(1) 564	E(1) 565	D(2) 566
8	G(2)	F(1)	E(1)
9	H(2)	G(2)	F(1)
10	Hold PCntr, Hold IR	Hold DR	G(2)
11	I(2)	H(2)	G(2)
12	Hold PCntr, Hold IR	Hold DR	H(2)
13	J(1)	I(2)	H(2)
14	Hold PCntr, Hold IR	Hold DR	I(2)
15	K(1)	J(1)	I(2)
16	L(1)	K(1)	J(1)
17	:	L(1)	K(1)
18	:	:	L(1)
19	:	:	:

Fig. 5

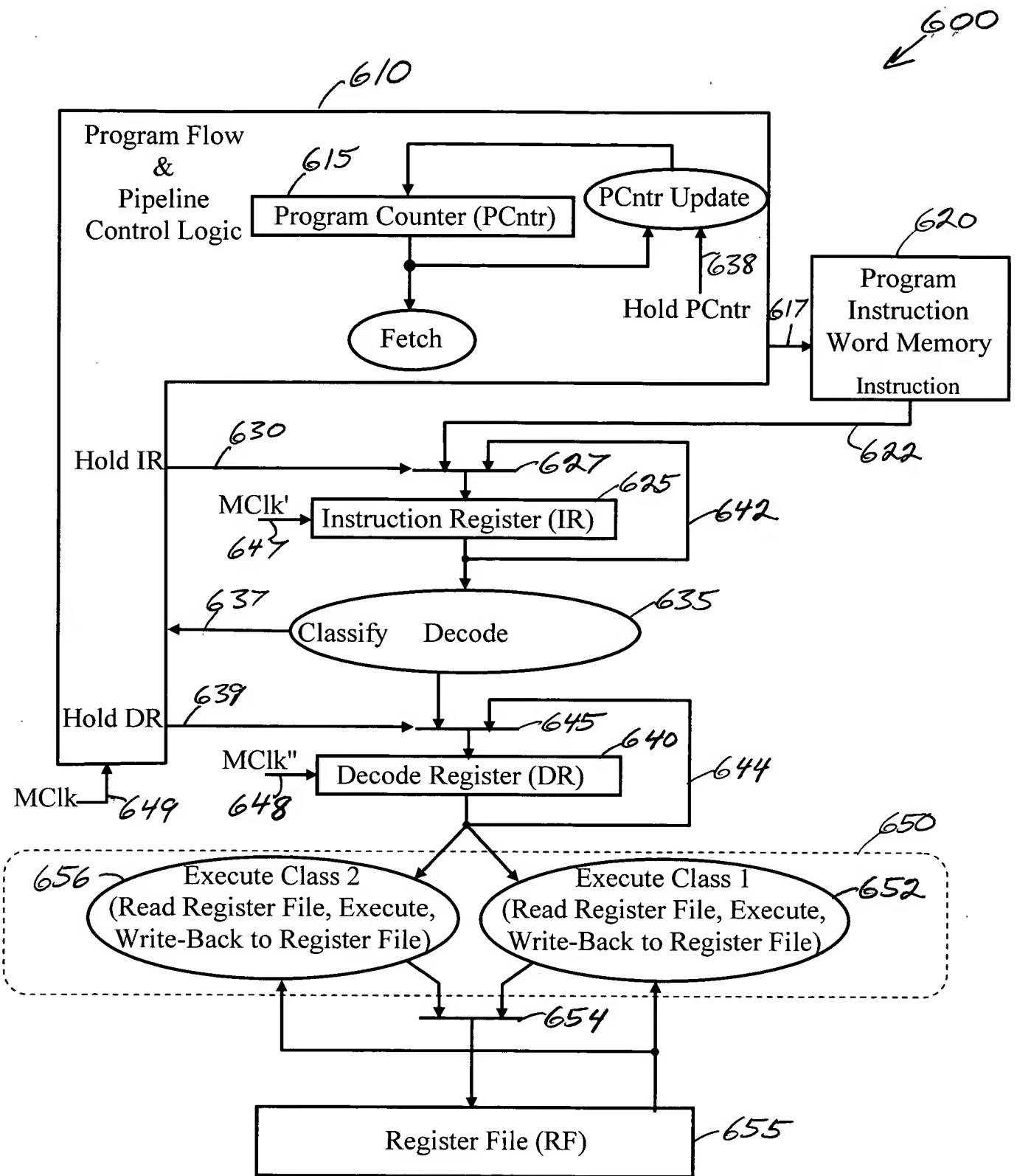


Fig. 6

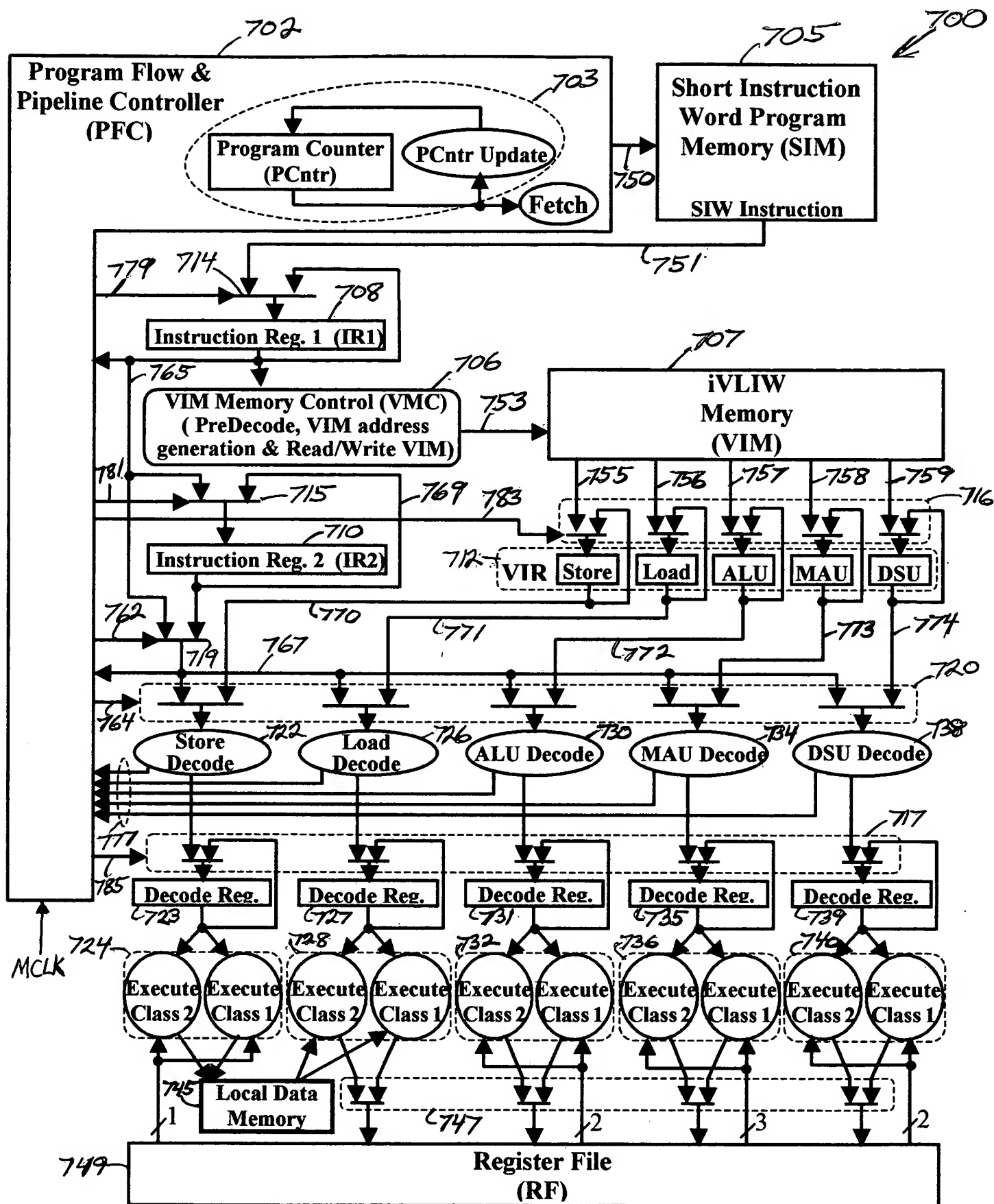


Fig. 7

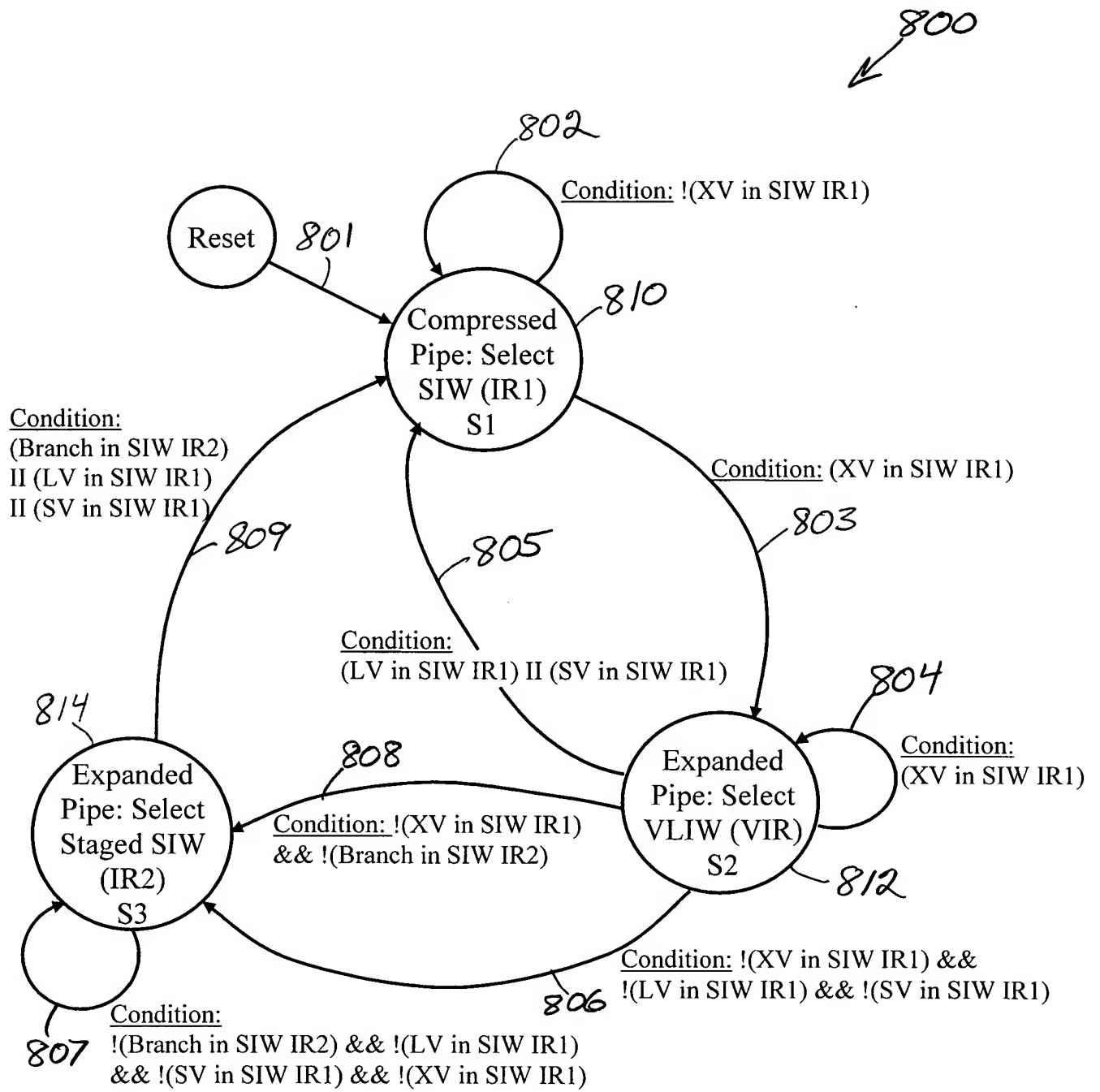
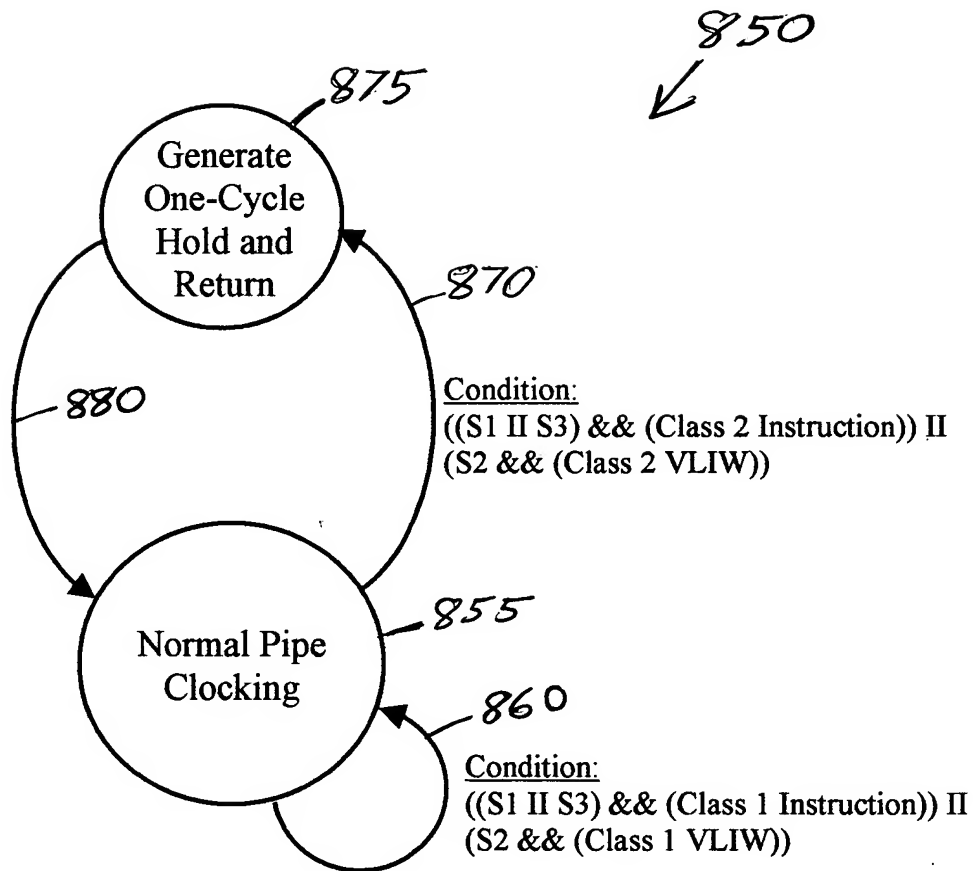


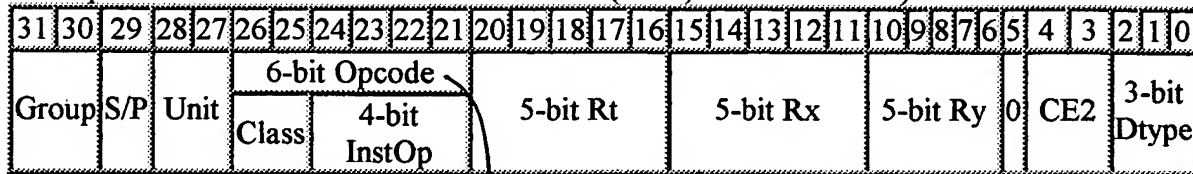
Fig. 8A



S1 = Compressed Pipe: Select SIW (IR1)
 S2 = Expanded Pipe: Select VLIW (VIR)
 S3 = Expanded Pipe: Select Staged SIW (IR2)
 Class 1 VLIW = All Enabled VLIW Slot Instructions are Class 1
 Class 2 VLIW = One or More Enabled VLIW Slot Instructions are Class 2

Fig. 8B

Example Basic Arithmetic Instruction Format (ALU, MAU and DSU)



0 0 = Class 1, PCLK = 3 MCLKs - 906

0 1 = Class 2, PCLK = 4 MCLKs - 908

1 0 = Class 3, PCLK = 6 MCLKs - 910

1 1 = Reserved - 912

Fig. 9A

925

MCLK Cycle #	PCLK Cycle #	Fetch	Decode	Execute
1 934	1 933	A(1) 932	:	:
2 935				
3 936				
4 940	2 937	B(2) 938	A(1) 939	:
5 941				
6 942				
7 947	3 943	C(3) 944	B(2) 945	A(1) 946
8 948				
9 949				
10 954	4 950	D(1) 951	C(3) 952	B(2) 953
11 955				
12 956				
13 957				
14 962	5 958	E(1) 959	D(1) 960	C(3) 961
15 963				
16 964				
17 965				
18 966				
19 967				
20 972	6 968	F(1) 969	E(1) 970	D(1) 971
21 973				
22 974				
23	7	:	:	:
24				
25				

Fig. 9B

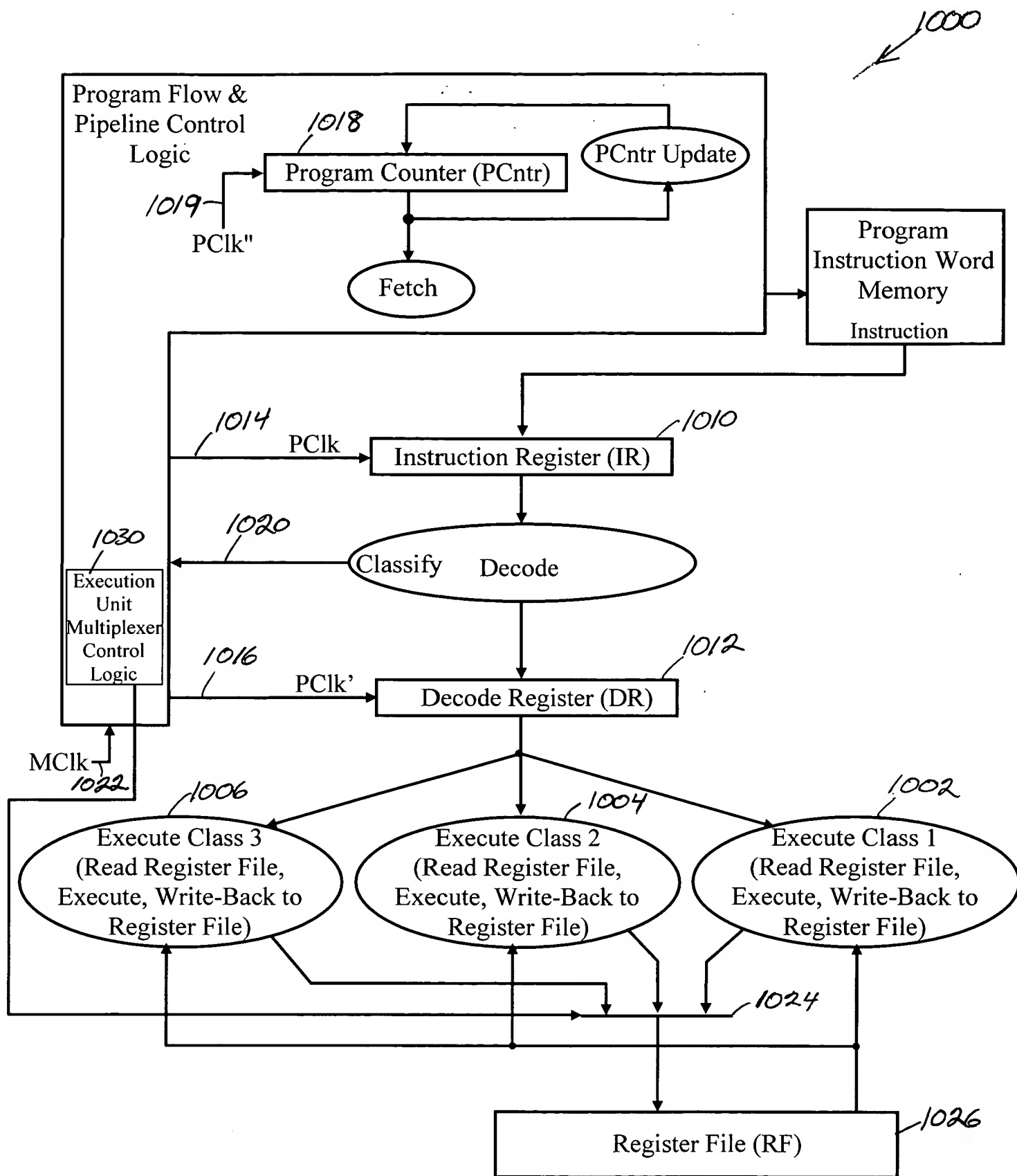


Fig. 10

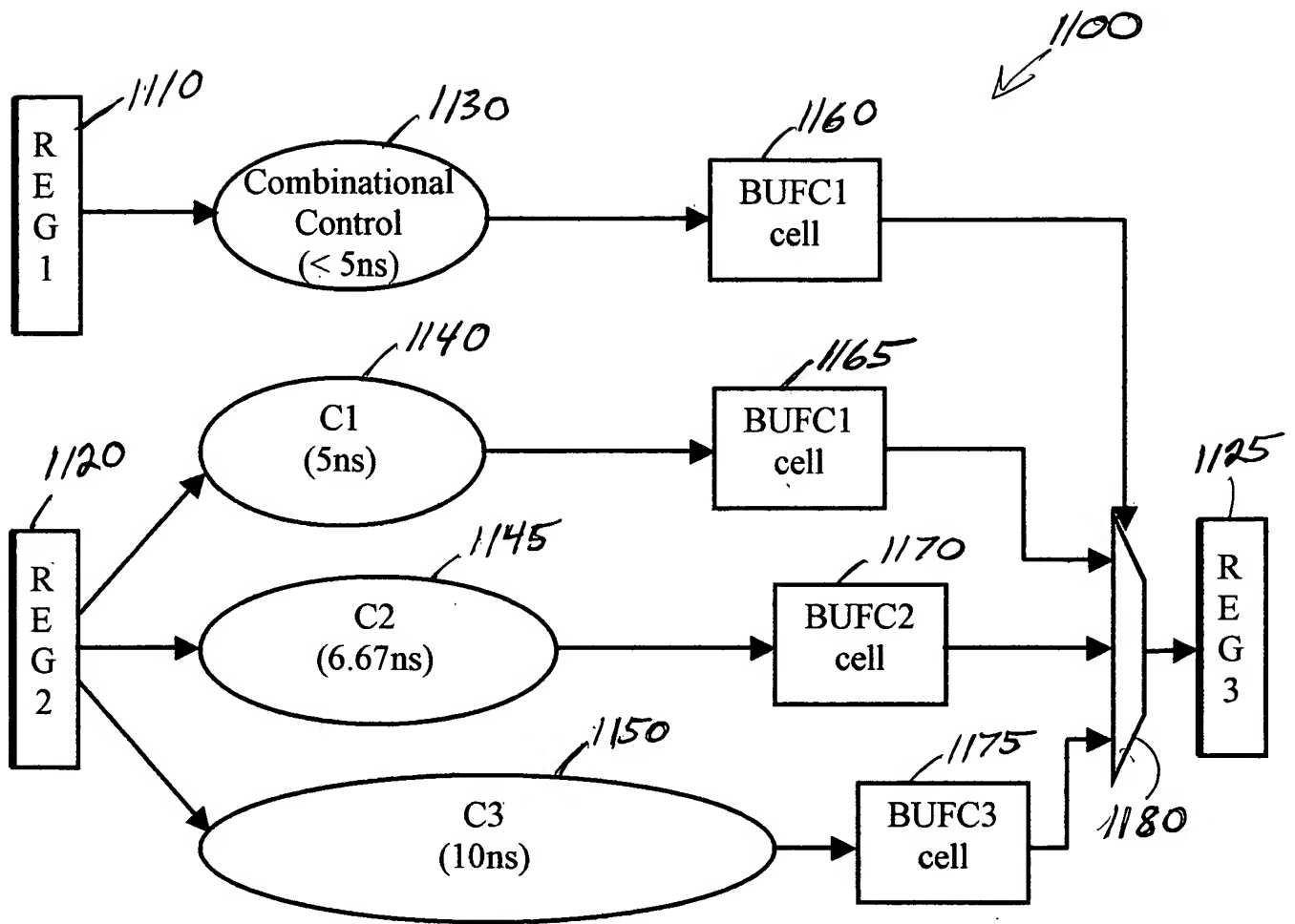


Fig. 11

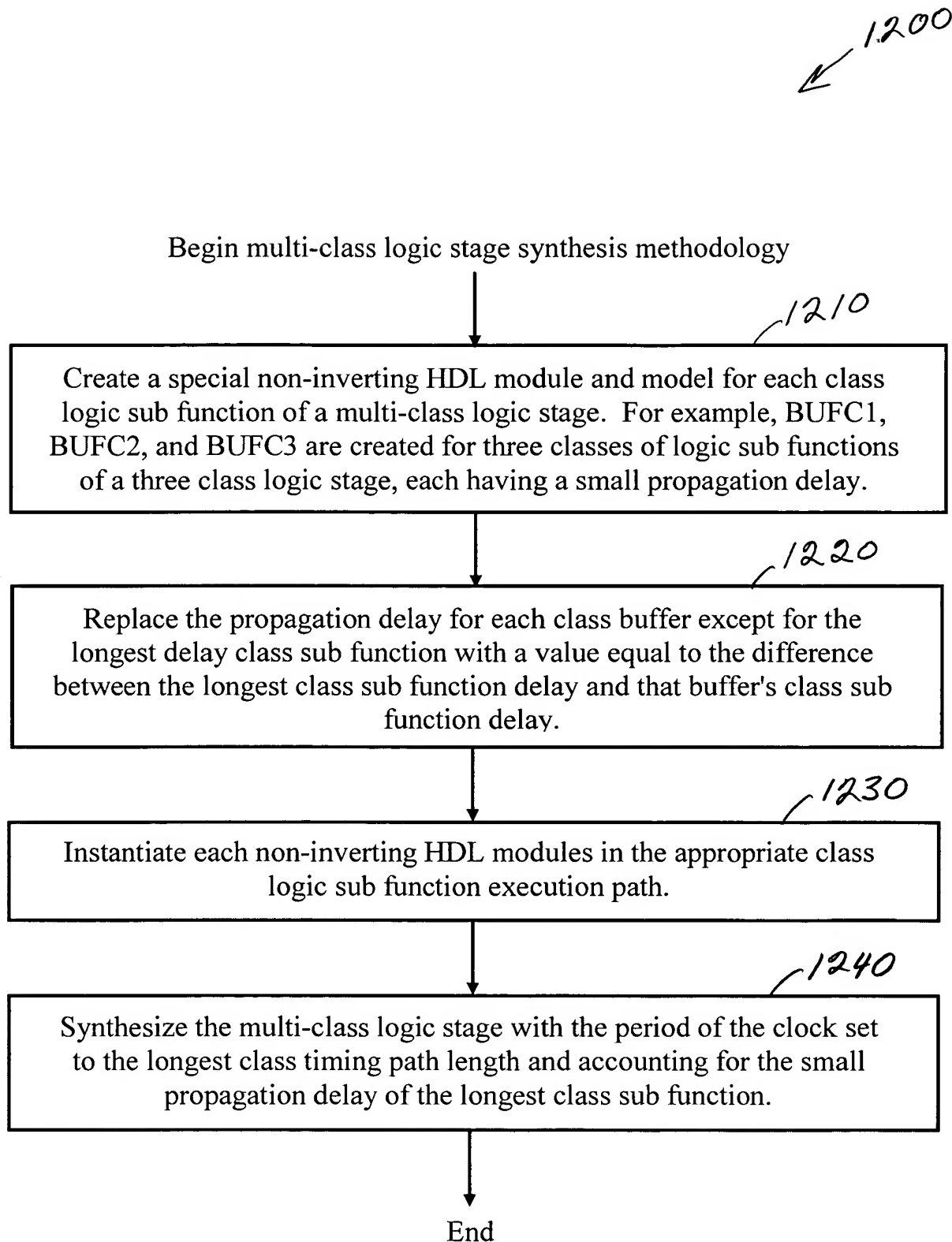


Fig. 12

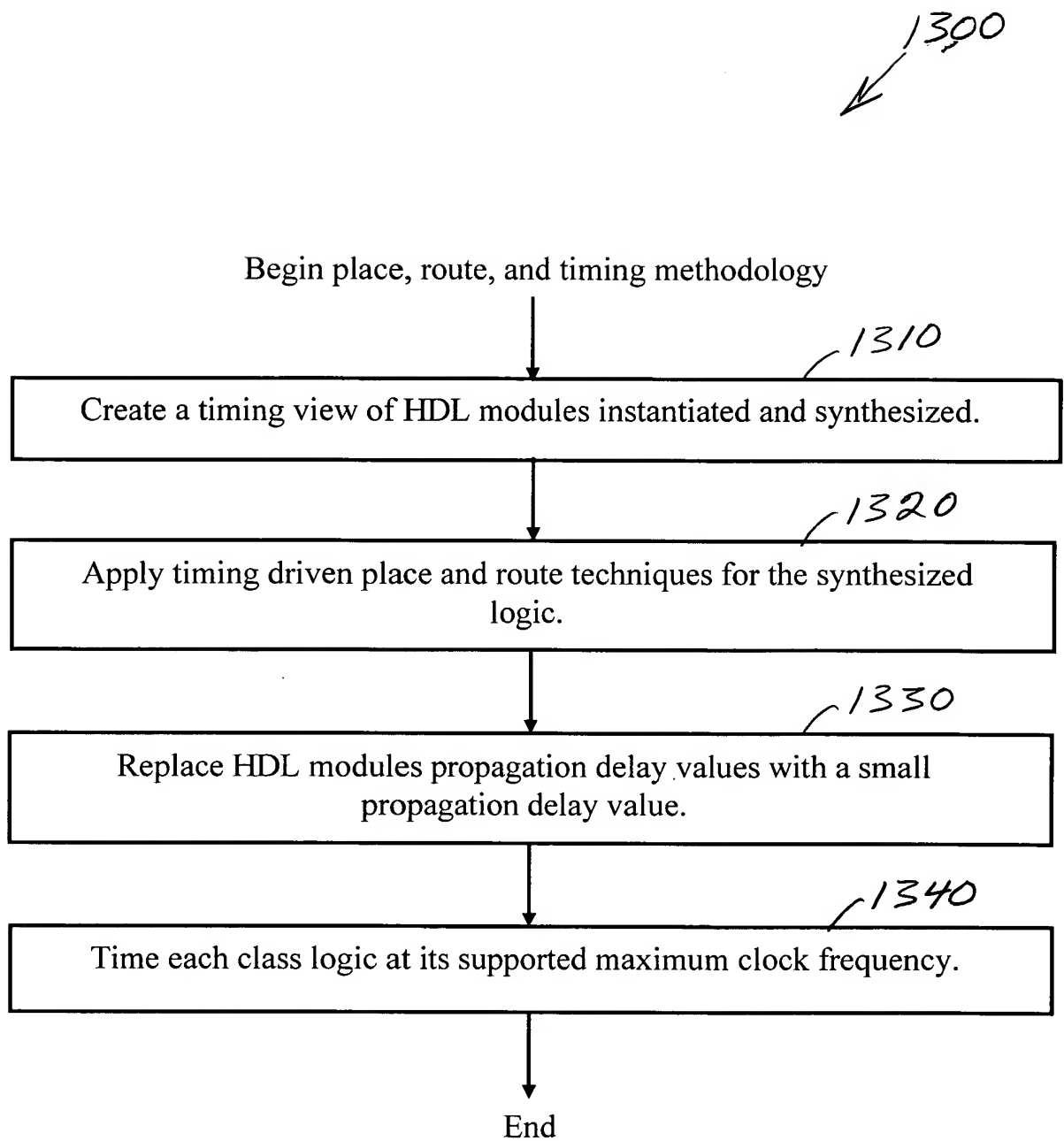


Fig. 13

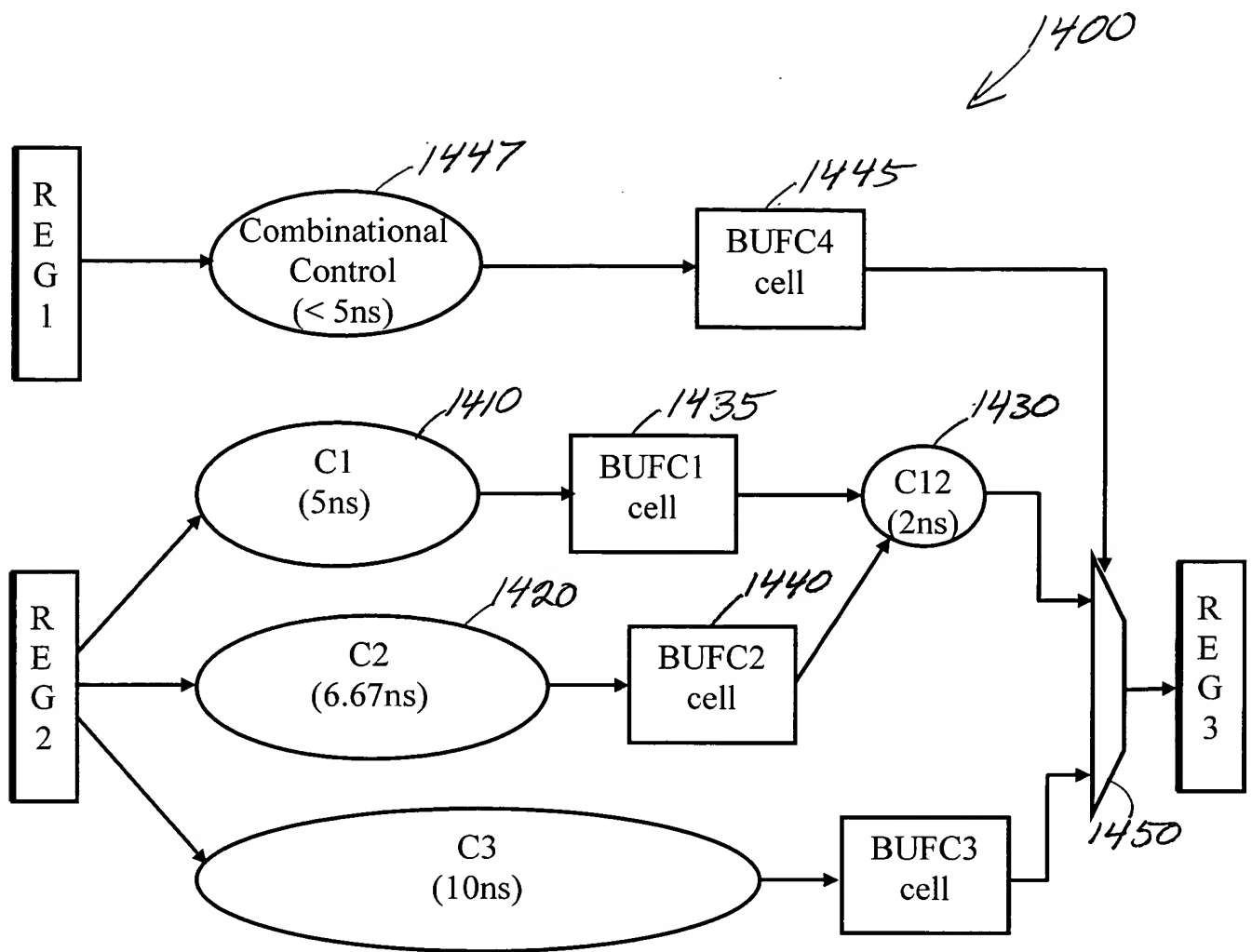


Fig. 14

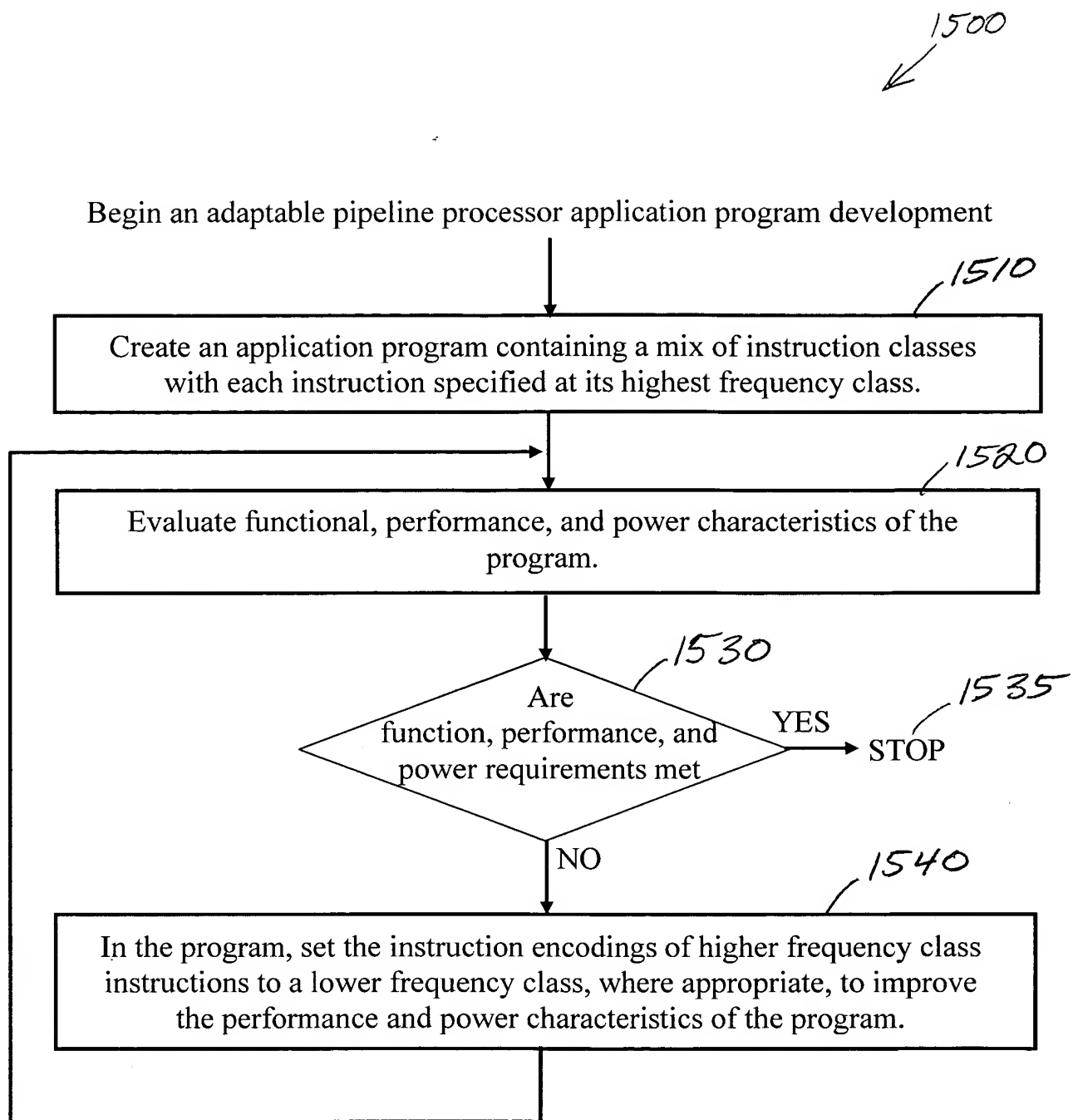


Fig. 15